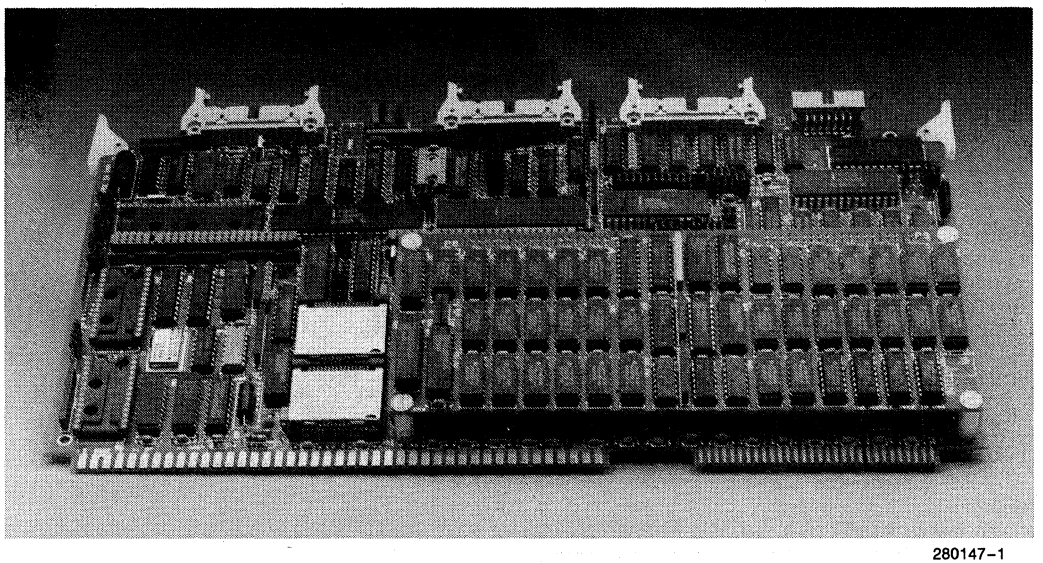
iSBC® 286/12, 286/14, 286/16 SINGLE BOARD COMPUTERS

- 8 MHz 80286 Microprocessor
- Two JEDEC 28-Pin Sites for up to 128K Bytes of Local EPROM Memory, Expandable to 256K Bytes Using an iSBC® 341 Expansion Module
- 1, 2, or 4 Megabyte, 0 Wait-State, Dual-Port, Parity Memory
- Supports User Installed 80287 Numeric Data Processor and 82258 Advanced DMA Controller Devices
- Two iSBX™ Bus Interface Connectors for I/O Expansion
- Synchronous High-Speed Interface for 0 Wait-State Read/Write to EX Memory Expansion Boards
- iLBX™ Interface for iLBX Memory Board Expansion
- 16 Levels of Vectored Interrupt Control
- Centronics-Compatible Parallel I/O Printer Interface
- Two Programmable Multiprotocol Synchronous/Asynchronous Serial Interfaces; One RS232C, the Other RS232C or RS422/449 Compatible

The iSBC 286/12, iSBC 286/14, and iSBC 286/16 Single Board Computers are members of Intel's high performance family of 16-bit microcomputers. The boards feature an 80286 microprocessor running at 8 MHz together with 1, 2, or 4 megabytes of dual-ported, 0 wait-state, parity memory. These features make the iSBC 286/12/14/16 boards the ideal single board solution for applications requiring high performance and up to 1, 2, or 4 megabytes of memory. For those applications needing more memory, up to four memory expansion boards may be connected to the iSBC 286/12/14/16 boards over its P2 interface. The P2 interface supports both standard iLBX memory boards and Intel's EX series of synchronous, 0 wait-state, memory boards that provide up to 16 megabytes of system memory. The iSBC 286/12/14/16 boards also feature two sockets for user installed 80287 Numeric Data Processor and 82258 Advanced Direct Memory Access Controller devices. These components further increase board performance by off-loading time intensive tasks from the 80286 microprocessor. The iSBC 286/12/14/16 CPU boards are true single-board solutions that also include two serial I/O channels, one parallel line printer channel, local memory, interrupt controllers and programmable timers all on one board.



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*XENIX is a registered trademark of Microsoft Corp.

**UNIX is a trademark of Bell Laboratories.

September 1986
Order Number: 280147-002

FUNCTIONAL DESCRIPTION

Overview

The iSBC 286/12/14/16 boards utilizes the powerful 80286 CPU within the MULTIBUS® system architecture, enhanced by the industry standard iLBX bus and a new, 0 wait-state, synchronous memory interface, to provide a high-performance 16-bit solution. This board features 1, 2, or 4 megabytes of dual-port, 0 wait-state, parity memory, plus interrupt, memory and I/O features facilitating a complete single-board computer system. The iSBC 286/12/14/16 boards can be used in many applications originally designed for Intel's other 16-bit microcomputers. Only minor changes to the system hardware or applications software may be required to match the application to the iSBC 286/12/14/16 boards. These changes may include adjusting software timing loops, changing the (jumper) default configuration of the board, and using pin and socket I/O connectors in place of edge connectors.

Central Processing Unit

The central processor for the iSBC 286/12/14/16 board is the 80286 CPU operating at an 8.0 MHz clock rate. The 80286 CPU is upwardly compatible with Intel's 8088 and 8086 CPUs. The 80286 CPU runs 8088 and 8086 code at substantially higher speeds due to its parallel architecture. In addition, the 80286 CPU provides on-chip memory management and protection and virtual memory addressing of up to 1 gigabyte per task. Processing speed and efficiency may be further enhanced by installing an 80287 numerics coprocessor and an 82258 ADMA controller. The clock rates for the 80286 and the 80287 are independent with the 80287 rate jumper selectable at either 5.3 MHz or 8.0 MHz.

Instruction Set

The 80286 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions.

Numeric Data Processor

For enhanced numerics processing capability, the 80287 Numeric Data Processor extends the 80286 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental,

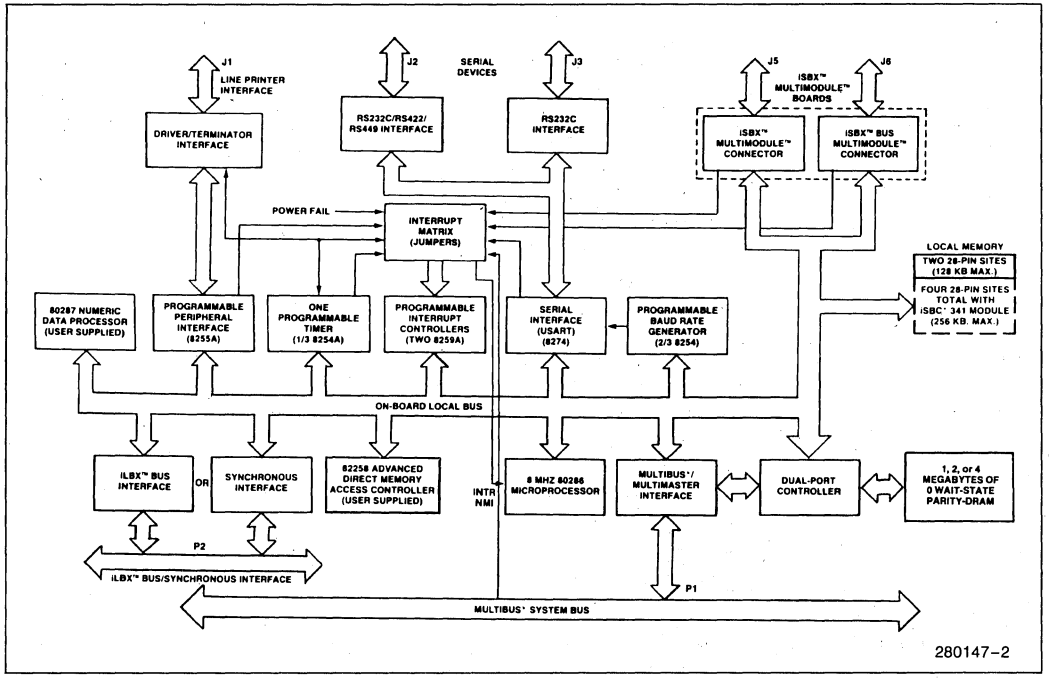

Figure 1. iSBC® 286/12 Block Diagram

logarithmic and exponential instructions. Supported data types include 16-, 32-, and 64-bit integer, 32- and 64-bit floating point, 18-digit packed BCD and 80-bit temporary. The 80287 meets the IEEE P754 standard for numeric data processing and maintains compatibility with 8087-based systems.

Advanced DMA Controller

For those applications that require frequent moving of large blocks of data, the user may install an Intel 82258, 4 channel, advanced DMA (ADMA) controller to further increase system performance. The ADMA Controller supports DMA requests from the 8274 USART (2 channels) and the iSBX interfaces on the board (1 per interface). The ADMA can also perform data transfers over the on-board CPU bus, the MULTIBUS (P1) interface, and the iLBX/synchronous (P2) interface. With this arrangement, the device can rapidly move blocks of data between the iSBC 286/12/14/16 boards and iSBX MULTIMODULE™ Boards installed on the baseboard, between the iSBC 286/12/14/16 boards and other boards installed in the system, or between any other memory/controller/I/O boards installed in the system.

ARCHITECTURAL FEATURES

The 8086, 8088, 80186 and 80286 microprocessor family contains the same basic set of registers, instructions, and addressing modes. The 80286 processor is upward compatible with the 8086, 8088, and 80186 CPUs.

The 80286 operates in two modes: 8086 real address mode, and protected virtual address mode. In 8086 real address mode, programs use real address with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same base instruction set and registers.

Vectored Interrupt Control

Incoming interrupts are handled by two on-board 8259A programmable interrupt controllers (PIC) and by the 80286's NMI line. Interrupts originating from up to 15 sources are prioritized and then sent to the CPU. The 8259 devices support both polled and vectored mode of operation. Further interrupt capability is available through bus vectored interrupts where slave 8259 interrupt controllers resident on separate iSBC Boards supply an interrupt vector to the on-board CPU.

Table 1. Interrupt Request Sources

Device	Function	Number of Interrupts
MULTIBUS Interface	Requests from MULTIBUS resident peripherals or other CPU boards	8*
8259A Programmable Interrupt Controller	8 level vectored interrupt request from slave 8259A	1
8274 Serial Controller	6 internal interrupt requests directed to master 8259A	1
8255A Line Printer Interface	Signals output buffer empty. Directed to slave PIC	1
8254 Timers	Timer 0, 1 outputs; function determined by timer mode	2
iSBX connectors	Function determined by iSBX MULTIMODULE board Directed to slave PIC	2 per iSBX Connector
Bus Fail Safe Timer	Indicates addressed MULTIBUS resident device has not responded to command within 10 ms	1
Power Fail Interrupt	Indicates AC power is not within tolerance (from power supply)	1
ADMA Interrupt	Common interrupt for 4 DMA channels	1
Parity Interrupt	Parity error indicator from memory module	1
On-Board Logic	Conditioned interrupt source from edge sense latch, inverter, or OR gate	3
Bus Request Error	Indicates CPU was unable to access the MULTIBUS interface	1
External Interrupt	Supports system front panel reset switch	1

NOTE:
*May be expanded to 56 with slave 8259A PICs on MULTIBUS boards.

Interrupt Sources

Twenty-six potential interrupt sources are routed to the slave PIC device and to the interrupt jumper matrix where the user can connect the desired interrupt sources to specific interrupt levels. Table 1 includes a list of devices and functions supported by interrupts.

Memory Capabilities

DUAL-PORT MEMORY

The iSBC 286/12/14/16 boards feature 1, 2, or 4 megabytes of 0 wait-state, parity memory installed on the board. This memory, which is implemented using 256 Kb or 1 Mb DRAMs installed on a daughter board, is dual-ported to the on-board CPU bus and the MULTIBUS (P1) interface. For those applications requiring more memory, the iSBC 286/12/14/16 boards also feature an iLBX and synchronous memory interface to increase physical memory capacity to 16 megabytes.

LOCAL MEMORY

Two, 28-pin sites are provided for installing up to 128 KB of EPROM firmware.

By installing an iSBC 341 EPROM expansion module, local memory can be increased to four sites to support up to 256 KB of EPROM. Local memory access time is selectable at one, two, or three wait-states and is a function of the speed of the devices used.

Serial I/O

A two-channel serial communications interface using Intel's 8274 Multi-Protocol Serial Controller (MPSC) is contained on the iSBC 286/12/14/16 boards. Two independent software selectable baud rate generators (⅔ of the 8254 timer) provide the MPSC with all common communication frequencies. The protocol (i.e. asynchronous, bisync, or SDLC/HDLC), data format, control character format, parity and baud rate are all under program control. Software interfacing to the MPSC can be via either a polled or interrupt driven routine. Channel A may be configured for an RS232C or RS422/RS449 interface; channel B is set for RS232C operation only. DMA operation for channel A is available if the optional 82258 (ADMA) is installed. The data, clock, control, and signal ground lines for each channel are brought out to two 26-pin, pin and socket connectors.

Programmable Timers

The iSBC 286/12/14/16 boards provide three independent, fully programmable 16-bit interval timers/event counters utilizing the Intel 8254 Programmable Interval Timer. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs of these counters is jumper selectable. The outputs may be independently routed to the 8259A Programmable Interrupt Controller or to the 8274 MPSC to count external events or provide baud rate generation. The third interval timer in the 8254 is dedicated to providing a clock for the programmable baud rate generator in the iSBC 286/12/14/16 boards' MPSC serial controller. The system software configures each timer independently to select the desired function. Seven functions are available as shown in Table 2. The contents of each counter may be read at any time during system operation.

Table 2. Programmable Timer Functions

Function	Operation
Interrupt on Terminal Count	When a terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge or software command and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Software Triggered Strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware Triggered Strobe	Outputs goes low for one clock period N counts after rising edge counter trigger input. The counter is retriggerable.
Event Counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counter "window" has been enabled or an interrupt may be generated after N events occur in the system.

Line Printer Interface/Board ID

An 8255A Programmable Peripheral Interface (PPI) provides a Centronics compatible line printer interface, several on-board functions, and four non-dedicated input bits. Drivers are provided for a complete Centronics compatible line printer interface. The on-board functions implemented with the PPI are Power Fail Sense, Lock Override, NMI Mask, Clear Timeout Interrupt, LED 1 and 4, Clear Edge Sense flop, and MULTIBUS interface directed interrupts (2). The PPI's I/O lines are divided into three eight bit ports; A, B, and C. The PPI must be programmed for mode 0 with ports A and C used as outputs and port B as input. A 16-bit write to Port B is used to set the iSBC 286/12/14/16 boards into 24 bit address mode.

Table 3. Parallel Port Bit Assignment

Port A—Output	
Bit	**Function**
0	Line Printer Data Bit 0
1	Line Printer Data Bit 1
2	Line Printer Data Bit 2
3	Line Printer Data Bit 3
4	Line Printer Data Bit 4
5	Line Printer Data Bit 5
6	Line Printer Data Bit 6
7	Line Printer Data Bit 7
Port B—Input	
Bit	**Function**
0	Board ID Bit 0
1	Board ID Bit 1
2	Board ID Bit 2
3	LPT Interrupt (Active High)
4	Line Printer ACK/(Active Low)
5	Power Fail Sense/(Active Low)
6	Line Printer Error (Active High)
7	Line Printer Busy (Active High)
Port C—Output	
Bit	**Function**
0	Line Printer Data Strobe (Active High)
1	Override/(0 = lock asserted)
2	NMI Mask (0 = NMI Enabled)
3	Clear Timeout Interrupt (Active High)
4	LED 0 (1 = On); Clear Edge Sense Flop/
5	MULTIBUS Interrupt 1 (Active High)
6	MULTIBUS Interrupt 2 (Active High)
7	LED 1 (1 = On); Clear Line Printer ACK Flop/(Active High)

Three jumpers on the iSBC 286/12/14/16 boards let the software determine, by examining bits 0, 1, and 2 of port B, the board type (iSBC 286/10A board or iSBC 286/12/14/16 board), and the presence of hardware options (82258 ADMA and 80287 Numeric Data Processor devices) installed on the board. The parallel port assignment is shown in Table 3.

Software Reset

The software reset feature allows the 80286 microprocessor to return to Real Address mode operation from PVAM under software control. The system reset line (INIT*) and the dual-port memory are not affected, and all I/O context is preserved. The software reset is activated by a byte write to I/O location 00E0H. To distinguish the software reset from a true system initialization reset, a flag is provided. Another flag is provided that indicates whether the iSBC 286/12/14/16 board hardware (not the 80286 device) is currently configured for PVAM or Real Address Mode.

Front Panel Connector—J4

A 14-pin connector is mounted on the top edge of the board and is designed to connect to the front panel and power supply of the system enclosure. Leads supported include Reset and Interrupt input lines from (conditioned) front panel switches, a Run signal to drive a front panel LED, a Power Fail Interrupt line that connects to the power supply, and extra power and ground leads to support miscellaneous front panel circuitry.

MULTIBUS® SYSTEM ARCHITECTURE

Overview

The MULTIBUS system architecture includes three bus structures: the system bus, the local bus extension and the iSBX MULTIMODULE expansion bus as shown in Figure 2. Each bus structure is optimized to satisfy particular system requirements. The system bus provides a basis for general system design including memory and I/O expansion as well as multiprocessing support. The local bus extension allows large amounts of high performance memory to be accessed from a CPU board over a private bus. The MULTIMODULE extension bus is a means of adding inexpensive I/O functions to a base CPU board. Each of these three bus structures are implemented on the iSBC 286/12/14/16 boards providing a total system architecture solution.

System Bus—IEEE 796

The MULTIBUS system bus is Intel's industry standard, IEEE 796, microcomputer bus structure. Both 8- and 16-bit single board computers are supported on the IEEE 796 structure with 24 address and 16 data lines. In its simplest application, the system bus allows expansion of functions already contained on a single board computer (e.g., memory and digital I/O). However, the IEEE 796 bus also allows very powerful distributed processing configurations using multiple processors, I/O boards, and peripheral boards. The MULTIBUS system bus is supported with a broad array of board level products, VLSI interface components, detailed published specifications and application notes.

System Bus—Expansion Capabilities

Memory and I/O capacity may be expanded and additional functions added using Intel MUTLIBUS compatible expansion boards. Memory may be expanded by adding user specified combinations of RAM boards, EPROM boards, bubble memory boards, or combination boards. Input/output capacity may be added with digital I/O and analog I/O expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers. Modular expandable backplanes and cardcages are available to support multiboard systems.

System Bus—Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically sharing system tasks through communication of the system bus), the iSBC 286/12/14/16 boards provide full system bus arbitration control logic. This control logic allows up to three iSBC 286/12/14/16 boards or other bus masters, including the iSBC 80 Board family of MULTIBUS compatible 8-bit single board computers to share the system bus using a serial (daisy

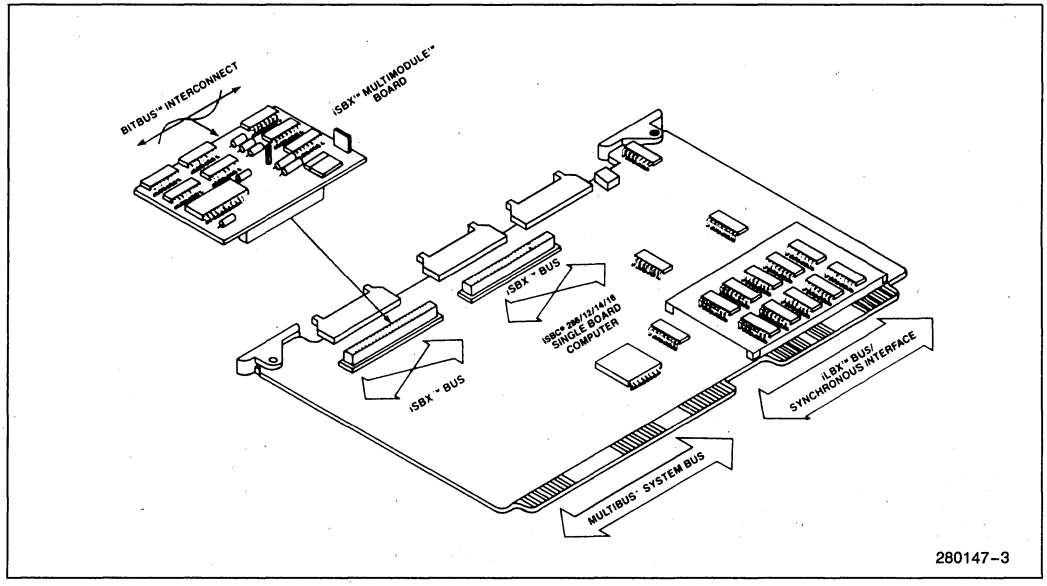

Figure 2. MULTIBUS® System Architecture

chain) priority scheme and allows up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to multiprocessing configuration made possible with multimaster capability, it also provides a very efficient mechanism for all forms of DMA (Direct Memory Access) transfers.

Memory Map

The memory map of the iSBC 286/12/14/16 board is shown in Figure 3. The memory maps for the iSBC 286/14 and iSBC 286/16 boards are similar, except the total amount of on-board DRAM memory is 2 or 4 MB, and the dual-port memory space is larger. The memory map, which shows the default configuration of the board, may be easily changed by the user to meet the needs of almost any system design. As a result, the iSBC 286/12/14/16 boards are particularly suited for complex multiple processor and/or multiple intelligent I/O board-based systems.

The memory map can be changed by moving on-board jumpers or by installing user-programmed PALs (programmable array logic devices).

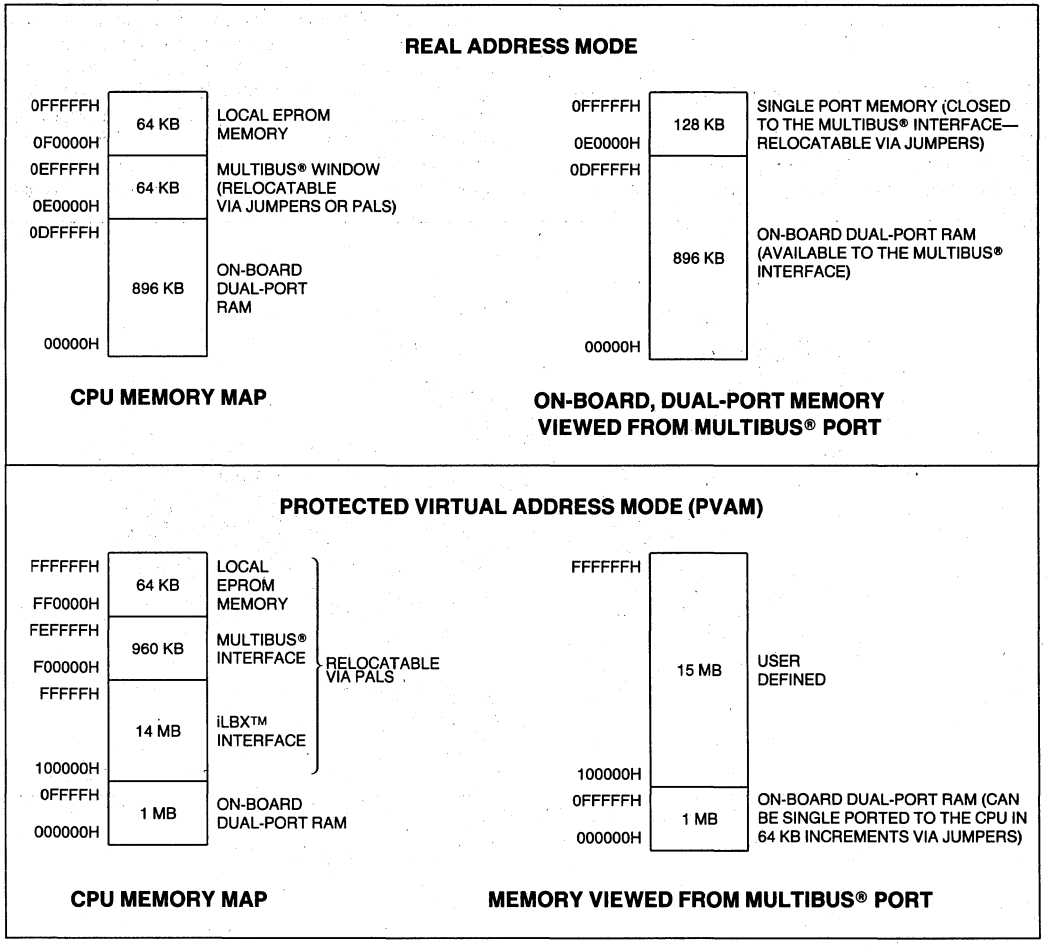

Figure 3. Memory Map for iSBC® 286/12 Board (Default Configuration)

Using only the jumpers on the iSBC 286/12/14/16 board, the MULTIBUS window size can be set at 0 (no window), 64 KB, 128 KB, 256 KB, or 1 MB in real address mode. The MULTIBUS window is normally not available in PVAM, however, a PAL may be programmed to provide this feature. Jumpers are also used to set aside a portion of the dual-port memory so that it may only be accessed by the CPU (single-ported memory). Block sizes of 64 KB, 128 KB, 256 KB, 512 KB or 1 MB may be selected. Finally, jumpers are used to select any of 6 EPROM memory sizes ranging from 4 KB (using 2716 devices) up to 256 KB (using 27512 devices and an iSBC 341 module).

If the user needs to alter the memory map further, five PALs on the baseboard are socketed and may be replaced by custom designed devices. Using programmed PALs, the designer can:

— Set the base DRAM memory starting address (as viewed by the 80286 microprocessor) at 0 (default configuration) or to any ½ megabyte boundary up through 16 MB (0 or 512 KB in real address mode).

— Set the base DRAM memory starting address (as viewed by other boards over the MULTIBUS interface) at 0 (default configuration) or to any megabyte boundary up through 16 MB (fixed at 0 in real address mode).

— Set single or multiple MULTIBUS windows as small as 64 KB or as large as 1 MB within the first megabyte of address space. MULTIBUS windowing can be enabled both in real address mode and PVAM. The window size can also be set at 0 (no window) so that the CPU can only access its own DRAM memory.

The jumper and PAL changes may be used in combination with each other. For example, jumpers can be installed to set EPROM address space and to exclusively allocate (single-port) a portion of the dual-port memory to the CPU. Then, PALs can be installed to establish two MULTIBUS windows of different sizes and to set the DRAM base starting addresses.

High Speed Off-Board Memory

The iSBC 286/12/14/16 boards can access off-board memory either over the MULTIBUS (P1) interface, or over the P2 interface as shown in Figure 4. Memory transfers over the P2 interface are faster because the CPU board doesn't have to arbitrate for access to the MULTIBUS interface.

Using the P2 interface, the iSBC 286/12/14/16 boards can be configured to operate with either a standard iLBX interface or with a high-performance, synchronous interface.

The iSBC 286/12/14/16 boards as supplied are configured to operate with a synchronous, P2 inter-

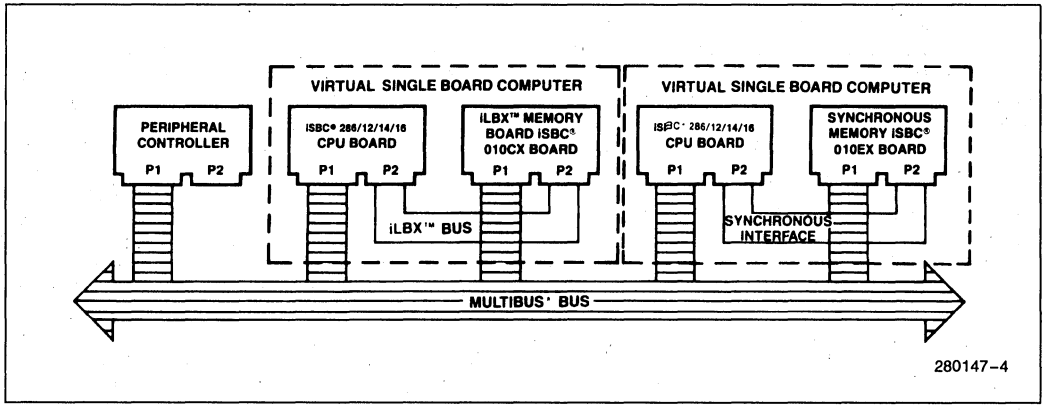

Figure 4. MULTIBUS®/iLBX™/Synchronous Interface Configurations

face. This high-performance interface is designed to connect to Intel's EX series of memory expansion boards to yield a CPU to memory read/write time of 0 wait-states. The EX memory expansion boards are available in sizes ranging from 512K bytes up to 4M bytes.

By moving several jumpers on the board, the iSBC 286/12/14/16 Single Board Computers may be reconfigured for an iLBX interface, and are compatible with Intel's CX series of memory expansion boards, which are available in sizes ranging from 512K bytes up to 2M bytes. Memory expansion boards from other manufacturers that meet the iLBX standard may also be used. CPU to memory access time is usually 1 or more wait-states depending on the speed of the memory used.

A total of four memory boards can be placed on the iLBX or synchronous interface bus. With 4M byte memory boards, this results in a total of 16M bytes on the memory expansion bus.

iSBX™ Bus MULTIMODULE™ On-Board Expansion

Two 8-, 16-bit iSBX MULTIMODULE connectors are provided on the iSBC 286/12/14/16 boards. Through these connectors, additional on-board I/O functions may be added. The iSBX MULTIMODULE Boards optimally support functions provided by VLSI peripheral components such as additional parallel and serial I/O, analog I/O, small mass storage device controllers (e.g., floppy disks), and other custom interfaces to meet specific needs. By mounting directly on the single board computer, less interface logic, less power, simpler packaging, higher performance, and lower cost result when compared to other alternatives such as MULTIBUS Board form factor compatible boards. The iSBX interface connectors on the iSBC 286/12/14/16 boards provide all signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. The iSBX MULTIMODULE Boards designed with 8-bit data paths and using the 8-bit iSBX connector are also supported on the iSBC 286/12/14/16 microcomputer boards. A broad range of iSBX MULTIMODULE Board options are available from Intel. Custom iSBX modules may also be designed. An iSBX bus interface specification is available from Intel.

SOFTWARE SUPPORT

Software support from Intel includes the iRMX 86, iRMX 286, and XENIX* Operating Systems, assembly and high level languages, development systems, in-circuit emulators, and various other hardware and software tools.

For those applications needing a real time, multitasking operating system, Intel offers the iRMX 86 Release 6 and iRMX 286 Release 1 Operating Systems. The iRMX operating systems are particularly well suited for industrial or commercial applications where the processor is simultaneously controlling multiple, real time, interrupt-intensive processes. Typical applications include machine and process control, data acquisition, signal processing, front-end processing, and digital PABX control. The iRMX operating systems employ a highly configurable, modular structure that allows easy system configuration and expansion.

The iRMX 86 Release 6 Operating System enables the iSBC 286/12/14/16 boards to address up to 1 MB of memory in real address mode. Using the iRMX 286 Operating System, this address range is extended to 16 MB in protected mode. The iRMX 286 Operating System also allows the user to take advantage of the hardware traps built into the iAPX 286 processor that provide expanded debug capabilities and increased code reliability.

Applications software written for earlier releases of the iRMX 86 Operating System is upwardly compatible through Release 6. Furthermore, application code written for the iRMX 86 Operating System can be compiled using 286 compilers to run under the iRMX 286 Operating System. Application code will require only minor changes.

Assembly and many high level languages are supported by the iRMX Operating Systems and Intellec® Series III and Series IV development systems. Language support for the iSBC 286/12/14/16 boards in real address mode includes Intel's ASM 86, PL/M 86, PASCAL 86, FORTRAN 86, and C86, as well as many third party 8086 languages. Language support for protected address mode include ASM 286, PL/M 286, PASCAL 286, and FORTRAN 286. Programs developed in these languages can be downloaded from an Intel Series III or IV Development System to the iSBC 286/12/14/16 boards via the iSDM™ 286 System Debug Monitor. The iSDM 286 monitor also provides on-target program debugging support including breakpoint and memory examination features.

Intel also offers the XENIX operating system which is designed for those applications needing an interactive, multiple user system. Typical applications include small business systems, software develop-

ment/engineering workstations, distributed data processing, communications, and graphics.

Intel's XENIX operating system is a fully licensed derivative of UNIX**, enhanced by Intel to provide device driver support for Intel board and component products plus other features that yield greater flexibility, increased reliability, and easier configurability. Intel's XENIX operating system has been optimized for use with the 80286 microprocessor and supports such features as on-chip memory management and protection which provide ease of portability and higher performance.

Applications software can be written in either Intel's FORTRAN, COBOL, or BASIC languages using a XENIX based, Intel 286/310 or 286/380 system, or by using an Intel iDIS™ Database Information System. The user can also select from a wide variety of existing third party languages and applications software.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, 32 or 40 bits

Data—8 or 16 bits

System Clock

CPU—8.0 MHz

Numeric Processor—5.3 MHz or 8.0 MHz (Jumper Selectable)

Cycle Time

Basic Instruction—8.0 MHz - 250 ns (assumes instruction in queue)

NOTE:
Basic instruction cycle is defined as the fastest instruction time (i.e. two clock cycles)

Dual-Port Memory

1, 2, or 4 megabyte, 0 wait-state, parity DRAM dual-ported to the on-board CPU bus and the MULTIBUS interface.

Local Memory

Number of sockets—two 28-pin JEDEC sites, expandable to 4 sites using iSBC 341 JEDEC Expansion Module

Maximum Size—128 KB expandable to 256 KB by installing an iSBC 341 EPROM Expansion Module. Memory size is set by jumpers on the iSBC 286/12/14/16 board.

Compatible Devices—EPROM, up to 64K x 8 (Intel 27512)

Off-Board Physical Memory

Operating System	Address Mode	Size
iRMX 86 Release 6 O.S.	Real	1 MB
iRMX 286 Release 1 O.S.	Protected	16 MB
XENIX Release 3 O.S.	Protected	16 MB

Socket provided for Intel 82258, 4 channel, advanced DMA controller. Data transfer rate = 4 MB per second (two cycle transfer mode, memory to memory); 2.67 MB per second (16-bit iSBX I/O to dual-port memory).

Interrupt Capacity

26 interrupt sources (total); 5 hard-wired to the 8259A PIC; 21 jumper selectable

Interrupt Levels—16 vectored requests using two 8259A devices and the 80286 microprocessor's NMI line

I/O Capability

Parallel — Line printer interface, on-board functions, and 3-bit board installed options code

Serial — Two programmable channels using one 8274 device

Timers — Three programmable timers using one 8254 device

Expansion— Two 8/16-bit iSBX MULTIMODULE connectors

Timers

Input Frequencies—1.23 MHz ±0.1% or 4.00 MHz ±0.1% (Jumper Selectable)

OUTPUT FREQUENCIES/TIMING INTERVALS

Function	Single Timer/Counter		Dual Timer/Counter (two timers cascaded)	
	Min	Max	Min	Max
Real-Time Interrupt	500 ns	53.3 ms	1.0 μs	58.2 min
Programmable One-Shot	500 ns	53.3 ms	1.0 μs	58.2 min
Rate Generator	18.8 Hz	2.0 MHz	0.000286 Hz	1 MHz
Square-Wave Rate Generator	18.8 Hz	2.0 MHz	0.000286 Hz	1 MHz
Software Triggered Strobe	500 ns	53.3 ms	1.0 μs	58.2 min
Hardware Triggered Strobe	500 ns	53.3 ms	1.0 μs	58.2 min
Event Counter	—	8.0 MHz	—	—

Interfaces

MULTIBUS Bus—All signals TTL compatible

iSBX Bus—All signals TTL compatible

iLBX Bus—All signals TTL compatible

Synchronous Interface—All signals TTL compatible

Serial I/O— Channel A: RS232C/RS422/RS449 compatible, DCE or DTE

Channel B: RS232C compatible, DCE

NOTE:
For RS422/RS449 operation, user supplied line drivers and resistor terminators must be installed.

Timer—All signals TTL compatible

Interrupt Requests—All TTL compatible

MULTIBUS® DRIVERS

Function	Type	Sink Current (mA)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	32
Bus Control	Open Collector	16/32

iLBX™ DRIVERS

Function	Type	Sink Current (mA)
Data	Tri-State	64
Address	Tri-State	24
Commands	Tri-State	24
Bus Control	TTL	24

Serial Communications Characteristics

Synchronous—5–8 bit characters; internal or HDLC/SDLC character synchronization; automatic sync insertion; even or odd parity

Asynchronous—5–8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection; even or odd parity

BAUD RATES

Synchronous—600, 1.2 KB, 2.4 KB, 4.8 KB, 9.6 KB, 19.2 KB, 38.4 KB, 56 KB, 76.8 KB, 154 KB, 307 KB, 615 KB.

Asynchronous—75, 150, 300, 600, 1.2 KB, 2.4 KB, 4.8 KB, 9.6 KB, 19.2 KB.

NOTE:
Baud rates are software selectable.

Physical Characteristics

Width: 12.00 in. (30.48 cm)

Height: 7.05 in. (18.00 cm)

Depth: 0.88 in. (2.24 cm)
1.16 in. (2.95 cm) with iSBX MULTIMODULE board installed

Recommended Slot spacing (without iSBX MULTIMODULE): 1.2 in. (3.0 cm)

Weight: 26 oz. (731 gm)

Mating Connectors (or Equivalent Part)

Function	# of Pins	Centers (In)	Connector Type	Vendor	Vendor Part No.
iSBX Bus Connector 16-Bit (J5, J6)	44	0.1	Soldered	Viking	000293-0001
I/O Connectors (J1–J3)	26	0.1	Flat Crimp	3M	3399-6026
Front Panel Connector (J4)	14	0.5	Flat Crimp	3M	3385-6014
iLBX/Synch. Interface Edge Connector (P2)	60	0.1	Flat Crimp	KEL-AM T & B Ansley	RF30-2803-5 A3020

Electrical Characteristics

DC Power Requirements:

Maximum: +5V, 8.7A; ±12V, 35 mA (for serial I/O)

Typical: +5V, 5.7A; ±12V, 20 mA

NOTE:
Power requirements are for the default configuration. Does not include power for optional EPROM, 80287 or 82258 devices, or installed iSBX MULTIMODULE boards.

Environmental Characteristics

Operating Temperature: 0°C to 60°C with 8 CFM airflow across board (default configuration)

Relative Humidity: to 90% (without condensation)

Reference Manual

147533— iSBC 286/12/14/16 Hardware Reference Manual (order separately)

ORDERING INFORMATION

Part Number Description

SBC 286/12	Single Board Computer with 1 MB of Memory
SBC 286/14	Single Board Computer with 2 MB of Memory
SBC 286/16	Single Board Computer with 4 MB of Memory
C80287-3	Numeric Processor Ext., 5 MHz
D80287-8	Numeric Processor Ext., 8 MHz
R82258-8	ADMA Coprocessor, 8 MHz