intel®

SYSTEM 80/20

A rack-mountable, packaged microcomputer for OEM applications

Processing power from the popular SBC 80/20 Single Board Computer.

Full multiprocessor bus control logic allows additional masters to share system bus

Eight-level programmable vectored priority interrupt control

Two programmable 16-bit BCD or Binary Timers

Auxiliary power bus and memory protect control logic provided for battery back-up RAM requirements

Expandable memory capacity

- 2K bytes RAM standard
- Expandable with low-cost 16K RAM, ROM, EPROM, and Combination Modules

Fully programmable I/O

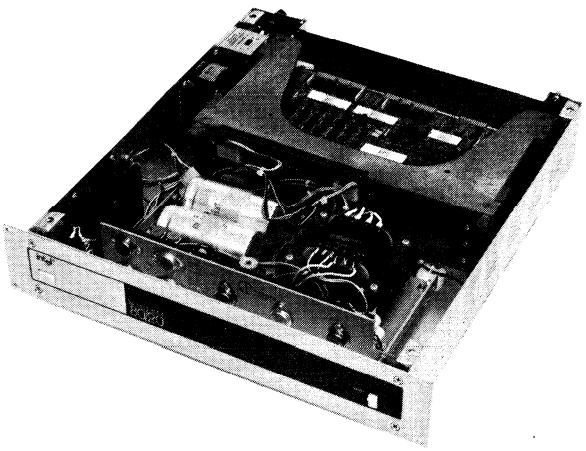
- Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rate generation
- 48 lines parallel I/O standard
- Expandable with low-cost I/O and Combination Modules

Comprehensive System Monitor for loading, execution, and debugging of System 80/20 programs

- Display and alter memory locations
- Display and alter registers
- Single-step program execution
- Read and Write paper tape commands
- RS232 driver

The System 80/20 is a fully packaged microcomputer utilizing the SBC 80/20 Single Board Computer. Ideal for the OEM whose design requires low-cost 19" RETMA compatible rack mountable packaging. The System 80/20 offers easy to use, fully programmable I/O, the computational power of the SBC 80/20, and has both RAM and EPROM memory. The enclosed power supply is designed to support not only the Single Board Computer, but also a full complement of expansion boards. The RETMA compatible chassis houses the computer, power supply, fans, and has three additional slots for expansion boards.

MICRO-COMPUTER SYSTEMS



The heart of the System 80/20 is the SBC 80/20 Single Board Computer, a complete computer on a single printed circuit board. The SBC 80/20 includes an 8080A CPU, 2K bytes of static RAM memory, sockets for 4K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous RS232C communications interface, programmable eight level vectored priority interrupt structure, programmable interval timers, and bus drivers for memory and I/O expansion.

Read-Only-Memory may be added in 1K byte increments using Intel® 8708 Erasable and Electrically Reprogrammable ROMs (EPROMs) or Intel® 8308 Masked ROMs. All on-board memory operations are performed at maximum processor speed.

Intel's powerful 8-bit, N-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the SBC 80/20. The 8080A contains six 8-bit general-purpose registers and an accumulator. The six general-purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out stack to store the contents of the program counter, flags, accumulator, and all of the six general-purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting that is bounded only by memory size.

The System 80/20 contains 48 programmable parallel I/O lines implemented using two Intel® 8255 Programmable Peripheral interfaces. The system software may configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application.

The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable, woven cable, or round cable. The user may design his own cables or order the SBC 955 Serial Cable or the SBC 956 Parallel Cable set.

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of the RS232C compatible interface on the board, allows the system to be used directly with CRTs, RS232C compatible cassettes, and asynchronous and synchronous modems. The RS232C command lines, serial data lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat- or round-cable. A 20-mil TTY compatible interface may be achieved by using the SBC 530 TTY Adapter.

The System 80/20 is a full computer with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the system bus), the System 80/20

TABLE 1

INPUT/OUTPUT PORT MODES OF OPERATION

PORTS	NO. OF LINES	MODE OF OPERATION					
		UNIDIRECTIONAL				BIDIRECTIONAL	CONTROL
		INPUT		OUTPUT			
		UNLATCHED	LATCHED & STROBED	LATCHED	LATCHED & STROBED		
1	8	X	X	X	X	X	
2	8	X	X	X	X		
3	4	X		X			X[1]
	4	X		X			X[1]
4	8	X	X	X	X	X	
5	8	X	X	X	X		
6	4	X		X			X[2]
	4	X		X			X[2]

NOTES:

1. Part of Port 3 must be used as a control port when either Port 1 or Port 2 are used as a latched and strobed input or a latched and strobed output port or Port 1 is used as a bidirectional port.
2. Part of Port 6 must be used as a control port when either Port 4 or Port 5 are used as a latched and strobed input or a latched and strobed output port or Port 4 is used as a bidirectional port.

provides full bus arbitration control logic. This control logic allows additional SBC 80/20s or other high-speed controllers to share the system bus in serial (daisy chain) priority fashion, or in parallel priority fashion with the addition of an external priority network. Once bus control is attained, a bus bandwidth of up to 5 Mbytes/sec may be achieved.

The bus controller provides its own clock which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data bytes per second.

The System 80/20 provides three fully programmable and independent BCD and binary 16-bit interval timers/event counters utilizing an Intel® 8253 Programmable Interval Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper-selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators or outputs from 8255 Programmable Peripheral Interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the RS232C USART serial port.

The systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timer/event counters select the desired function. Five functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple READ operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly."

An Intel® 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage via software, of a single byte to the Interrupt Mask Register on the PIC.

The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32 or 64-byte block may be located to begin at any 32 or 64-byte boundary in the 65,536 byte memory space. A single 8080A

TABLE 2

PROGRAMMABLE TIMER FUNCTIONS

FUNCTION	OPERATION
Interrupt on Terminal Count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of REAL-TIME CLOCKS.
Programmable One-Shot	Output goes low upon receipt of an external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate Generator	Divide by N counter. The output will go low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square-Wave Rate Generator	Output will remain high until one-half the count has been completed, and go low for the other half of the count.
Event Counter	On a jumper-selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.

TABLE 3

PROGRAMMABLE INTERRUPT MODES

MODE	OPERATION
FULLY NESTED	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
AUTO-ROTATING	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
SPECIFIC PRIORITY	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
POLLED	System software examines priority-encoded system interrupt status via Interrupt Status Register.

JUMP instruction at each of these addresses can then provide linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt requests may originate from 26 sources. Four jumper-selectable interrupt requests can be automatically generated by the Programmable Peripheral Interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper-selectable interrupt requests can be automatically generated by the USART when a character

is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper-selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the system bus.

System 80/20 memory may be increased by adding combinations of SBC 016 16K RAM boards and SBC 416 16K PROM boards. Input/Output capacity may be increased using the SBC 508 parallel I/O, the SBC 517 programmable serial and parallel I/O, or the SBC 519 programmable parallel I/O board. System resources may be increased simultaneously using SBC 80 combination I/O and memory expansion boards. All combination boards provide 48 lines of programmable parallel I/O, one programmable serial port, and sockets for up to 4K of EPROM. A RAM increment of 4K, 8K, or 16K can be chosen with the SBC 104, 108, or 116, respectively.

Mass storage capacity may be added to the System 80/20 with Intel's Flexible Diskette peripherals. The SBC 201 Diskette Controller is a very powerful and easy to use plug-in module which is compatible with several manufacturers' diskette drives. For a completely tested mass storage peripheral, the SBC 211 Single Drive System and the SBC 212 Dual Drive System are available.

A Modular Cardcage/Backplane is installed in the chassis to house the SBC 80/20 and provide an easily accessible bus interface. The cardcage houses the SBC 80/20 and any additional expansion boards. All SBC 80 bus signals are present on all mating connectors. Also included are power supply cables which mate with the power supply connectors on the backplane to carry ±5V and ±12V DC.

A comprehensive system monitor, residing in two Intel ROMs, is included to facilitate the loading, execution, and debug of programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display and alter memory contents, display and alter CPU register contents, and single step program execution.

Monitor commands and resulting information may be initiated and displayed using a CRT or other RS232 device.

The System 80/20 is designed for easy modular servicing. The computer boards are accessible from the rear of the package and strain relief clamps are included to protect any I/O cabling added by the OEM.

The System 80/20 comes with all in-depth documentation needed to program and interface with the system. An 8080 Assembly Language Manual, PL/M-80™ Programming Manual, and a Hardware Reference Manual, are all included to provide clear and concise information relevant to the use of a System 80/20.

The development cycle of System 80/20 based products may be significantly reduced using the Intellec® Microcomputer Development System. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. Optional Diskette Operating Software for the Development System programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique In-Circuit Emulator (ICE-80) option provides the capability to use the Development System to develop and debug software directly on the System 80/20.

Intel's high-level resident programming language, PL/M-80, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M-80 programs can be written in a much shorter time than assembly language programs.

SPECIFICATIONS

WORD SIZE
Instruction: 8, 16, or 24 bits
Data: 8 bits

CYCLE TIME
Basic Instruction Cycle: 1.86 μsec
Note: Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

MEMORY ADDRESSING
On-Board ROM/PROM: $0–0FFF_H$
On-Board RAM: 2K segments ending at any jumper-selectable address on a 16K boundary (e.g., 0000_H, 4000_H, . . . $C000_H$).

MEMORY CAPACITY
On-Board ROM/PROM: 4K bytes (sockets only)
On-Board RAM: 2K bytes
Off-Board Expansion: Up to 65,536 bytes in user-specified combinations of RAM, ROM, and PROM.
Note: ROM/PROM may be added in 1K byte increments.

I/O ADDRESSING
On-Board Programmable I/O (see Table 1).

Port	8255 No. 1			8255 No. 2			8255 No. 1 Control	8255 No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O CAPACITY
Parallel: 48 programmable lines (see Table 1).
Note: Expandable with optional I/O boards.

SERIAL COMMUNICATIONS CHARACTERISTICS
Synchronous:
5–8 bit characters
Internal or external character synchronization
Automatic Sync Insertion
Asynchronous:
5–8 bit characters
Break character generation
1, 1½, or 2 stop bits
False start bit detectors

SERIAL BAUD RATES

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)		
	Synchronous	Asynchronous (Program Selectable)	
		÷ 16	÷ 64
153.6	——	9600	2400
76.8	——	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
6.98	6980	——	110

Note: Frequency selected by I/O write of appropriate 16-bit frequency factor to Baud Rate Register.

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Register Address (Hex notation, I/O address space)

Baud Rate Register	DE

Note: Baud Rate Factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

INTERRUPTS

Register Address (Hex notation, I/O address space)

Interrupt Request Register	DA
In-Service Register	DA
Mask Register	DB
Command Register	DA
Block Address Register	DB
Status (Polling Register)	DA

Note: Several registers have the same physical address, sequence of access and one data bit of control word determines which register will respond.

TIMERS

Register Address Hex notation, I/O address space)

Control Register	DF
Timer 0	DC
Timer 1	DD

Note: Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies:

Reference: 1.0752 MHz ±0.1% (0.930 μsec period, nominal)
Event Rate: 1.1 MHz max

Note: Maximum rate for external events in Mode 4: Event Counter.

Output Frequencies/Timing Intervals:

Mode	Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
		Min.	Max.	Min.	Max.
0	Real-Time Interrupt	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
1	Programmable One-Shot	1.86 μsec	60.948 msec	3.72 μsec	1.109 hrs
2	Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
3	Square-Wave Rate Generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz

INTERFACES

Bus: All signals TTL compatible
Parallel I/O: All signals TTL compatible
Interrupt Requests: All TTL compatible
Timer: All signals TTL compatible
Serial I/O: RS232C compatible, data set configuration

SYSTEM CLOCK (8080A CPU)

2.154 MHz ±0.1%

COMPATIBLE CONNECTORS

Interface	No. of Double-Sided Pins	Centers (in.)	Mating Connectors
Parallel I/O (2)	50	0.1	3M 3415-000 Flat TI H312125 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat TI H312113

PHYSICAL CHARACTERISTICS

Height: 8.90 cm (3.5 in.)
Width: At Front Panel: 48.3 cm (19 in.)
Behind Front Panel: 43.2 cm (17 in.)
Depth: 50.8 cm (20 in. with all protrusions)

ELECTRICAL CHARACTERISTICS

Input Power:
Frequency: 47–63 Hz
Voltage: Standard: 115 VAC ±10%
Option: 230 VAC ±10%

Output Power Available for Expansion Boards:

Voltage	Supply Current	Power Available without PROM & Termination Packs Installed	Power Available with PROM & Termination Packs Installed*	Over Voltage Protection	RAM-Only Power Requirements
+12	2A	1.63A	1.45A	+14 to +16 volts	0.96A
+5	14A	9.1A	8.7A	5.8 to 6.6 volts	
–5	0.9A	0.72A	0.54A	5.8 to –6.6 volts	
–12	0.8A	0.77A	0.775A	–14 to –16 volts	

*PROMs are four 8708s; Termination Packs are eight 220Ω/330Ω Terminator Packs.

AUXILIARY POWER

An Auxiliary Power Bus is provided to allow separate power to RAM for systems requiring battery back-up of read/write memory. Selection of this Auxiliary RAM Power Bus is made via jumpers on the board.

MEMORY PROTECT

An active-low TTL compatible MEMORY PROTECT signal is brought out on the Auxiliary connector which, when asserted, disables Read/Write access to RAM memory on the board. This input is provided for the protection of RAM contents during system power-down sequences.

LINE DRIVERS AND TERMINATORS

I/O Drivers:

The following line drivers are all compatible with the I/O driver sockets on the SBC 80/20.

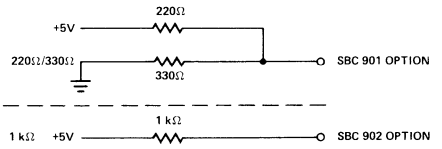
Driver	Characteristic	Sink Current (mA)
7438	I,OC	48
7437	I	48
7432	NI	16
7426	I,OC	16
7409	NI,OC	16
7408	NI	16
7403	I,OC	16
7400	I	16

Note: I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole dividers and 1 kΩ terminators.

I/O Terminators:

Terminators: 220Ω/330Ω divider or 1 kΩ pull-up.



Bus Drivers:

Function	Characteristic	Sink Current (mA)
Data	3-State	50
Address	3-State	50
Commands	3-State	32

ENVIRONMENTAL

Operating Temperature: 0°C to 50°C

SYSTEM MONITOR

Address:

$0000–069C_H$ (ROM), $3F80_H–3FFF_H$ (RAM)

Commands:

Display Memory (D)
Program Execute (G)
Insert Instruction into Memory (I)
Move Memory (M)
Execute Next Instruction (N)
Read Hexadecimal File (R)
Substitute Memory (S)
Write Hexadecimal File (W)
Examine and Modify CPU Registers (X)

Drivers:
- Console Input
- Console Output
- Reader Input
- Punch Output

Breakpoints:

Program BREAKing may occur upon any of up to seven system conditions. BREAKs are implemented via the Programmable Interrupt Controller. When a break occurs, the BREAK level, all CPU registers, and the next instruction (OP CODE) are displayed at the console.

Baud Rate:

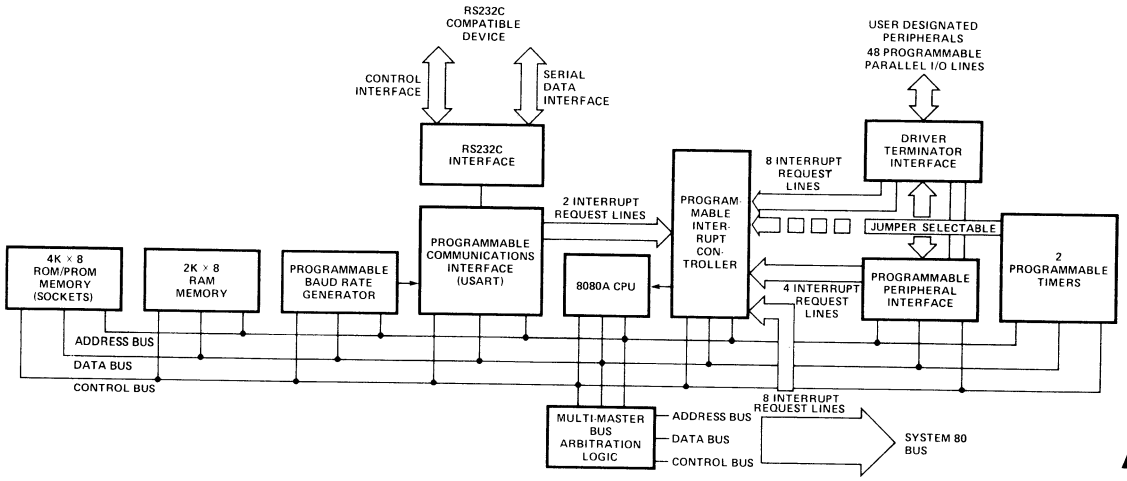
Baud Rate Search Capability automatically sets serial baud rate to that of the system console. Allowable baud rates include 110, 150, 300, 600, 1200, 2400, 4800, and 9600.

EQUIPMENT SUPPLIED
- System 80/20 Computer with power supply, cardcage, dual fans, and ROM based system monitor
- 115-volt power cable
- 115-volt and 230-volt fuses
- 8080 Assembly Language Manual
- PL/M-80 Programming Manual
- System 80/20 Hardware Reference Manual
- SBC 80/20 Schematics

COMPATIBLE BOARDS
- SBC 016 16K byte RAM
- SBC 104 4K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 108 8K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 116 16K bytes RAM, 4K bytes PROM, 48 programmable I/O lines, USART
- SBC 416 16K byte PROM
- SBC 501 DMA Controller
- SBC 508 32 input lines/32 output lines
- SBC 517 Combination I/O Board
- SBC 519 Programmable Parallel I/O Board
- SBC 955 Serial I/O Cable Set
- SBC 956 Parallel I/O Cable Set

COMPATIBLE PERIPHERALS
- SBC 201 Diskette Controller
- SBC 211 Single Diskette System
- SBC 212 Dual Diskette System

COMPATIBLE HARDWARE
- SBC 530 Teletypewriter Adapter



SYSTEM 80/20 BLOCK DIAGRAM