



SYSTEM 80/20-4

A rack mountable, packaged microcomputer for OEM applications

Processing power from the popular iSBC 80/20-4 Single Board Computer

Fully programmable I/O

- Programmable synchronous/asynchronous RS232C compatible serial interface with software selectable baud rate generation
- 48 lines parallel I/O standard
- Expandable with low cost digital I/O and analog I/O modules

Full MULTIBUS control logic allowing additional masters to share system bus

Two programmable 16-bit BCD or binary timers

Eight-level programmable vectored priority interrupt control

Expandable memory capacity

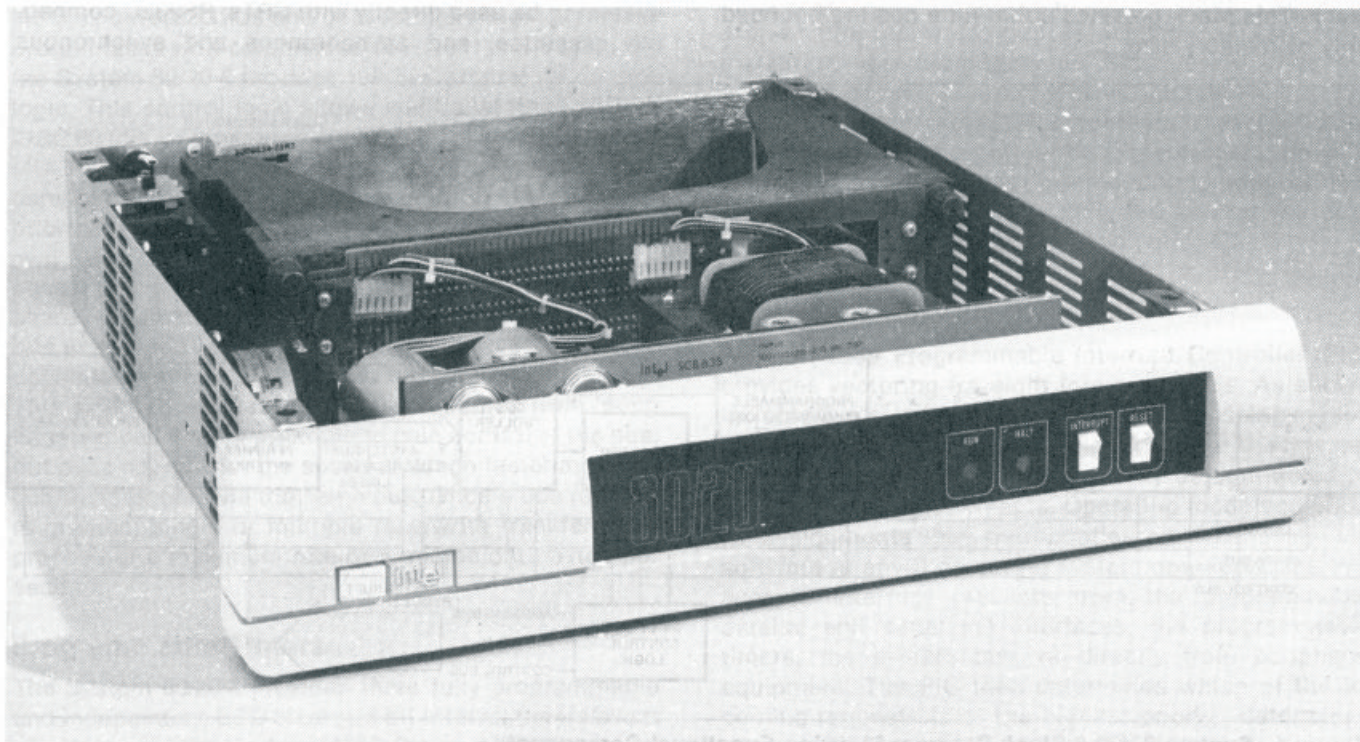
- 4K bytes RAM standard
- 8K EPROM capacity
- Expandable with low cost RAM, ROM, EPROM, and combination modules

Comprehensive system monitor for loading, executing, and debugging System 80/20-4 programs

- Display and alter memory locations
- Display and alter registers
- Single step program execution
- Read and write paper tape commands
- RS232C driver

The Intel System 80/20-4 is a fully packaged microcomputer utilizing the iSBC 80/20-4 Single Board Computer. Ideal for the OEM whose design requires low cost 19-inch RETMA compatible rack mountable packaging, the System 80/20-4 offers easy to use, fully programmable I/O and the computational power of the iSBC 80/20-4, and has both RAM and EPROM memory. The enclosed power supply is designed to support not only the single board computer, but also a full complement of expansion boards. The RETMA compatible chassis houses the computer, power supply, and fans, and has three additional slots for expansion.

PACKAGED
SYSTEMS



FUNCTIONAL DESCRIPTION

The heart of the System 80/20-4 is the iSBC 80/20-4 Single Board Computer, a complete computer on a single printed circuit board. The iSBC 80/20-4 includes an 8080A CPU, 4K bytes of static RAM memory, sockets for up to 8K bytes of EPROM memory, 48 programmable parallel I/O lines with sockets for interchangeable line drivers and terminators, a programmable synchronous/asynchronous RS232C communications interface, programmable 8-level vectored priority interrupt structure, programmable interval timers, and bus drivers for memory and I/O expansion. Read only memory may be added in 1K-byte increments using Intel 8708 erasable and electrically reprogrammable ROMs (EPROMs) or Intel 8308 masked ROMs, and in 2K-byte increments using Intel 8716 EPROMs or 8316B masked ROMs. All on-board memory operations are performed at maximum processor speed. A block diagram of the System 80/20-4 functional components is shown in Figure 1.

Memory Addressing

Intel's powerful 8-bit, N-channel MOS 8080A CPU, fabricated on a single LSI chip, is the central processor for the iSBC 80/20-4. The 8080A contains six 8-bit general purpose registers and an accumulator. The six general purpose registers may be addressed individually or in pairs, providing both single and double precision operations.

Memory Capacity

The 8080A has a 16-bit address bus which allows direct addressing of up to 64K bytes of memory. An external stack, located within any portion of read/write memory, may be used as a last-in/first-out storage area for the contents of the program counter, flags, accumulator, and all of the six general purpose registers. A 16-bit stack pointer controls the addressing of this external stack. This stack provides subroutine nesting bounded only by memory size.

Parallel I/O Interface

The System 80/20-4 contains 48 programmable parallel I/O lines implemented using two Intel 8255 programmable peripheral interfaces. The system software may configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. Therefore, the I/O interface may be customized to meet specified peripheral requirements. In order to take full advantage of the large number of possible I/O configurations, sockets are provided for interchangeable I/O line drivers and terminators. Hence, the I/O interface is further enhanced by the capability of selecting the appropriate combination of optional line drivers and terminators to provide the required sink current, polarity, and drive/termination characteristics for each application. The 48 programmable I/O lines and signal ground lines are brought out to two 50-pin edge connectors that mate with flat cable, woven cable, or round cable. The user may design his own cables or order the iSBC 956 Parallel I/O Cable Set.

Serial I/O Interface

A programmable communications interface using Intel's 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is contained on the board. A software selectable baud rate generator provides the USART with all common communications frequencies. The USART can be programmed by software to determine the desired asynchronous or synchronous serial data transmission technique (including IBM Bi-Sync). The mode of data transmission, data format, control character format, parity, and asynchronous transmission rate are all under program control. The 8251 provides full duplex, double buffered transmit and receive capability. Parity, overrun, and framing error detection are all incorporated in the USART. The inclusion of the RS232C compatible interface on the board allows the system to be used directly with CRTs, RS232C compatible cassettes, and asynchronous and synchronous

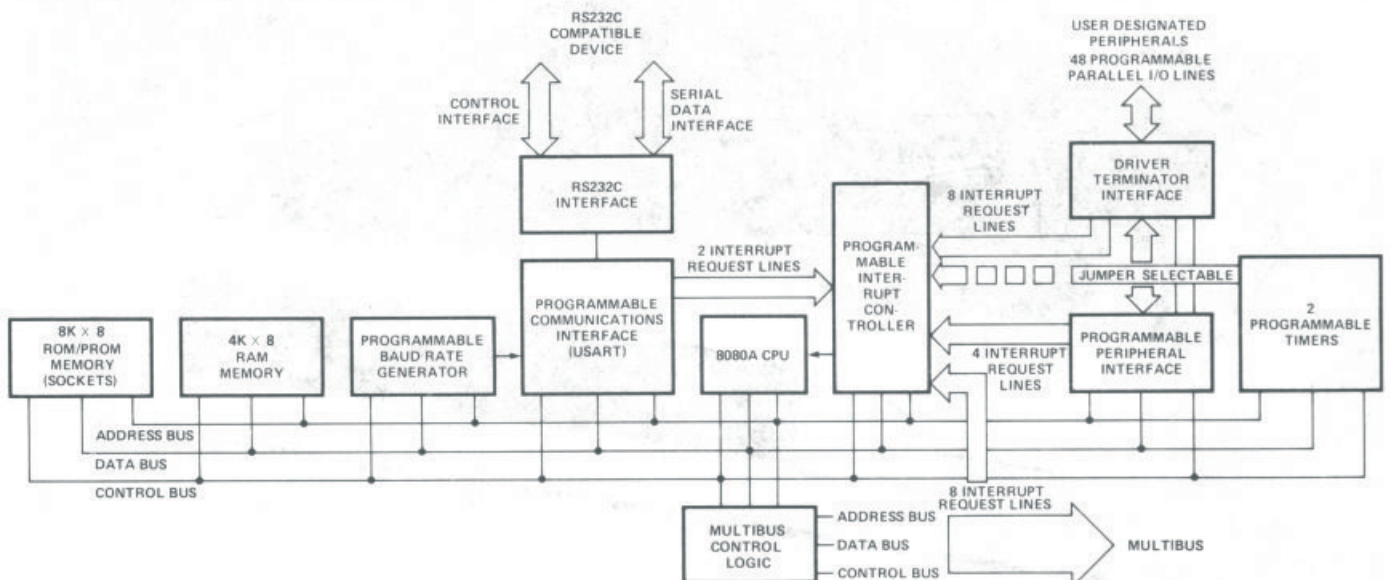


Figure 1. System 80/20-4 Block Diagram Showing Functional Components

Port	Lines (qty)	Mode of Operation				Control	
		Unidirectional					Bidirectional
		Input		Output			
		Unlatched	Latched & Strobed	Latched	Latched & Strobed		
1	8	X	X	X	X		
2	8	X	X	X	X		
3	4	X		X		X ¹	
	4	X		X		X ¹	
4	8	X	X	X	X		
5	8	X	X	X	X		
6	4	X		X		X ²	
	4	X		X		X ²	

Notes

1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a latched and strobed output port or port 1 is used as a bidirectional port.
2. Part of port 6 must be used as a control port when either port 4 or port 5 are used as a latched and strobed input or a latched and strobed output port or port 4 is used as a bidirectional port.

Table 1. Input/Output Port Modes of Operation

modems. The RS232C command lines, serial lines, and signal ground lines are brought out to a 26-pin edge connector that mates with RS232C compatible flat cable. A 20-mil TTY compatible interface may be achieved by using the optional ISBC 530 TTY Adapter.

Multimaster Capability

The System 80/20-4 is a full computer with resources capable of supporting the majority of OEM system requirements. For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e., several CPUs and/or controllers logically share system tasks with communication over the MULTIBUS), the System 80/20-4 provides full bus arbitration control logic. This control logic allows additional ISBC 80/20s, ISBC 80/05s, or other high speed controllers to share the MULTIBUS in serial (daisy chain) priority fashion, or in parallel priority fashion with the addition of an external priority network. The MULTIBUS controller provides its own clock, which is derived independently from the processor clock. This allows different speed controllers to share resources on the same bus, and transfers via the bus to proceed asynchronously. Thus, transfer speed is dependent on transmitting and receiving devices only. This design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed at a maximum rate of 5 million data bytes per second.

Programmable Timers

The System 80/20-4 provides three fully programmable and independent BCD binary 16-bit interval timers/event counters utilizing an Intel 8253 Programmable Interval

Timer. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing for the outputs and gate/trigger inputs of each of these counters is jumper selectable. Each may be independently routed to the programmable interrupt controller, the I/O line drivers and terminators, or the outputs from 8255 programmable peripheral interfaces. The third interval timer in the 8253 provides the programmable baud rate generator for the RS232C USART serial port. The systems designer simply configures, via software, each timer independently to meet system requirements. Whenever a given time delay or count is needed, software commands to the programmable timers/event counters select the desired function. Seven functions are available, as shown in Table 2. The contents of each counter may be read at any time during system operation with simple read operations for event counting applications, and special commands are included so that the contents of each counter can be used "on the fly".

Interrupt Capability

An Intel 8259 Programmable Interrupt Controller (PIC) provides vectoring for eight interrupt levels. As shown in Table 3, a selection of four priority processing modes is available to the systems designer so that the manner in which requests are processed may be configured to match system requirements. Operating mode and priority assignments may be reconfigured dynamically via software at any time during system operation. The PIC accepts interrupt requests from the programmable parallel and serial I/O interfaces, the programmable timers, the system bus, or directly from peripheral equipment. The PIC then determines which of the incoming requests is of the highest priority, determines whether this request is of higher priority than the level

currently being serviced, and if appropriate, issues an interrupt to the CPU. Any combination of interrupt levels may be masked through storage (via software) of a single byte to the interrupt mask register of the PIC.

Function	Operation
Interrupt on terminal count	When terminal count is reached, an interrupt request is generated. This function is extremely useful for generation of real-time clocks.
Programmable one-shot	Output goes low upon receipt of an external trigger edge and returns high when terminal count is reached. This function is retriggerable.
Rate generator	Divide by N counter. The output goes low for one input clock cycle, and the period from one low-going pulse to the next is N times the input clock period.
Square wave rate generator	Output remains high until one-half the count has been completed, and goes low for the other half of the count.
Event counter	On a jumper selectable basis, the clock input becomes an input from the external system. CPU may read the number of events occurring after the counting "window" has been enabled or an interrupt may be generated after N events occur in the system.
Software triggered strobe	Output remains high until software loads count (N). N counts after count is loaded, output goes low for one input clock period.
Hardware triggered strobe	Output goes low for one clock period N counts after rising edge on counter trigger input. The counter is retriggerable.

Table 2. Programmable Timer Functions

Interrupt Addressing — The PIC generates a unique memory address for each interrupt level. These addresses are equally spaced at intervals of 4 or 8 (software selectable) bytes. This 32- or 64-byte block may be located to begin at any 32- or 64-byte boundary in the 65,536-byte memory space. A single 8080A jump instruction at each of these addresses can then provide linkage to locate each interrupt service routine independently anywhere in memory.

Interrupt Request Generation — Interrupt requests may originate from 26 sources. Four jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). Two jumper selectable interrupt requests can be automatically generated by the USART when a character

is ready to be transferred to the CPU (i.e., receive channel buffer is full) or a character is ready to be transmitted (i.e., transmit channel data buffer is empty). A jumper selectable request can be generated by each of the programmable timers. Nine additional interrupt request lines are available to the user for direct interfaces to user designated peripheral devices via the MULTIBUS. BUS.

Function	Operation
Fully nested	Interrupt request line priorities fixed at 0 as highest, 7 as lowest.
Auto-rotating	Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.
Specific priority	System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.
Polled	System software examines priority -encoded system interrupt status via interrupt status register.

Table 3. Programmable Interrupt Modes

Expansion Capabilities

System 80/20-4 memory may be increased by adding combinations of iSBC RAM boards and iSBC PROM boards. Input/output capacity may be increased using the iSBC digital I/O or analog I/O boards. System resources may be increased simultaneously using iSBC 80 combination and I/O and memory expansion boards. All combination boards provide 48 lines of programmable parallel I/O, one programmable serial port, and sockets for up to 8K of EPROM. A RAM increment of 4K, 8K, or 16K can be chosen with the iSBC 104, 108, or 116, respectively.

Peripherals — Mass storage capacity may be added to the System 80/20-4 with Intel's flexible diskette peripherals. The iSBC 201 Single Density Diskette Controller and iSBC 202 Double Density Diskette Controller are powerful and easy to use plug-in modules which are compatible with several manufacturers' diskette drives. For a completely tested mass storage peripheral, the iSBC 211 single drive system and the iSBC 212 dual drive system are available.

Bus Interface — A modular cardcage/backplane is installed in the chassis to house the iSBC 80/20-4 and provide an easily accessible bus interface. The cardcage also houses any additional expansion boards. All iSBC 80 bus signals are present on all mating connectors. Also included are power supply cables which mate with the power supply connectors on the backplane to carry $\pm 5V$ and $\pm 12V$ DC.

System Monitor

A comprehensive system monitor, residing in two Intel 1K-byte ROMs, is included to facilitate loading, executing, and debugging programs. Monitor commands include the ability to read and write hexadecimal paper tapes, execute predefined program segments, display

and alter memory contents, display and alter CPU register contents, and execute single step programs. Monitor commands and resulting information may be initiated and displayed using CRT or other RS232C device.

Real-Time Software

The System 80/20-4 is totally compatible with Intel's RMX/80 Real-Time Multi-Tasking Executive. User programs (tasks) can take advantage of RMX/80 to do all necessary scheduling, intertask communication, and memory space allocation. RMX/80 also provides standard I/O support software such as the disk file handler, the Intel analog board handler, and the terminal handler.

System Development Capability

The development cycle of System 80/20-4-based products may be significantly reduced using an Intel microcomputer development system. The resident macroassembler, text editor, and system monitor greatly simplify the design, development, and debug of the system software. Optional diskette operating software for the development system allows programs to be loaded, assembled, edited, and executed faster than using conventional paper tape, card, or cassette peripherals. A unique in-circuit emulator (ICE-80) option

provides the capability to use the development system to develop and debug software directly on the System 80/20-4.

PL/M-80 Programming Capability

Intel's high level resident programming language, PL/M-80, provides the capability to program in a natural, algorithmic language and eliminates the need to manage register usage or allocate memory. PL/M-80 programs can be written in a much shorter time than assembly language programs.

Service Accessibility

The System 80/20-4 is designed for easy modular serviceability. The computer boards are accessible from the rear of the package and strain relief clamps are included to protect any I/O cabling added by the OEM. The power supply may be removed from the system to allow easy backplane servicing. An RS232C cable and connector are included as standard.

Support Documentation

The System 80/20-4 comes with all in-depth documentation needed to program and interface with the system. An 8080 assembly language manual and a hardware reference manual are included to provide clear and concise information relevant to the use of a System 80/20-4.

SPECIFICATIONS

Word Size

Instruction — 8, 16, or 24 bits

Data — 8 bits

Cycle Time

Basic Instruction Cycle — 1.86 μ s

Note

Basic instruction cycle is defined as the fastest instruction (i.e., four clock cycles).

Memory Addressing

On-Board ROM/EPROM — 0-0FFF_H

On-Board RAM — 4K segments ending at any jumper selectable address on a 16K boundary (e.g., 0000_H, 4000_H, ... C000_H).

Memory Capacity

On-Board ROM/EPROM — 8K bytes (sockets only)

On-Board RAM — 4K bytes

Off-Board Expansion — Up to 65,536 bytes in user specified combinations of RAM, ROM, and EPROM.

Note

ROM/EPROM may be added in 1K- or 2K-byte increments.

I/O Addressing

On-Board Programmable I/O — see Table 1

Port	8255A No. 1			8255A No. 2			8255A No. 1 Control	8255A No. 2 Control	USART Data	USART Control
	1	2	3	4	5	6				
Address	E4	E5	E6	E8	E9	EA	E7	EB	EC	ED

I/O Capacity

Parallel — 48 programmable lines (see Table 1)

Note

Expandable with optional I/O boards.

Serial Communications Characteristics

Synchronous — 5-8 bit characters; internal or external character synchronization; automatic sync insertion.

Asynchronous — 5-8 bit characters; break character generation; 1, 1½, or 2 stop bits; false start bit detection.

Baud Rates

Frequency (kHz) (Software Selectable)	Baud Rate (Hz)	
	Synchronous	Asynchronous
153.6	—	+ 16 9600 2400
76.8	—	4800 1200
38.4	38400	2400 600
19.2	19200	1200 300
9.6	9600	600 150
4.8	4800	300 75
6.98	6980	— 110

Note

Frequency selected by I/O write of appropriate 16-bit frequency factor to baud rate register.

Register Address (hex notation, I/O address space)

DE Baud rate register

Note

Baud rate factor (16 bits) is loaded as two sequential output operations to same address (DE_H).

Interrupts

Register Address (hex notation, I/O address space)

DA Interrupt request register
 DA In-service register
 DB Mask register
 DA Command register
 DB Block address register
 DA Status (polling register)

Note

Several registers have the same physical address; sequence of access and one data bit of control word determines which register will respond.

Timers

Register Address (hex notation, I/O address space)

DF Control register
 DC Timer 0
 DD Timer 1

Note

Timer counts loaded as two sequential output operations to same address, as given.

Input Frequencies

Reference	Event Rate
1.0752 MHz $\pm$ 0.1% (0.930 μ s period, nominal)	1.1 MHz ¹

Note

1. Maximum rate for external events in event counter function.

Output Frequencies/Timing Intervals

Function	Single Timer/Counter		Dual Timer/Counter (Two Timers Cascaded)	
	Min	Max	Min	Max
Real-time interrupt	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Programmable one-shot	1.86 μ s	60.945 ms	3.72 μ s	1.109 hr
Rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Square-wave rate generator	16.407 Hz	537.61 kHz	0.00025 Hz	268.81 kHz
Software triggered strobe	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr
Hardware triggered strobe	1.86 μ s	60.948 ms	3.72 μ s	1.109 hr

Interfaces

Bus — All signals TTL compatible

Parallel I/O — All signals TTL compatible

Interrupt Requests — All TTL compatible

Timer — All signals TTL compatible

Serial I/O — RS232C compatible, data set configuration

System Clock (8080A CPU)

2.154 MHz $\pm$ 0.1%

Physical Characteristics

Height — 3.5 in. (8.90 cm)

Width — At front panel — 19 in. (48.3 cm); behind front panel — 17 in. (43.2 cm)

Depth — 20 in. (50 cm) with all protrusions

Compatible Connectors

Interface	Double-Sided Pins (qty)	Centers (in.)	Mating Connectors
Parallel I/O (2)	50	0.1	3M 3415-000 Flat TI H312125 Flat
Serial I/O	26	0.1	3M 3462-0001 Flat TI H312113

Line Drivers and Terminators

I/O Drivers — The following line drivers are all compatible with the I/O driver sockets on the iSBC 80/04:

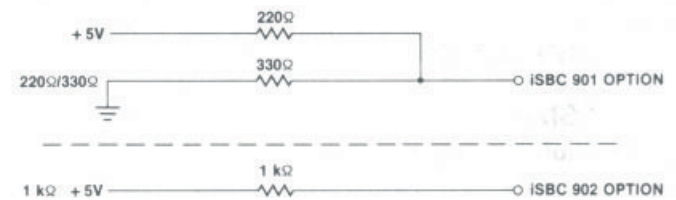
Driver	Characteristic	Sink Current (mA)
7438	I, OC	48
7437	I	48
7432	NI	16
7426	I, OC	16
7409	NI, OC	16
7408	NI	16
7403	I, OC	16
7400	I	16

Note

I = inverting; NI = non-inverting; OC = open collector.

Ports 1 and 4 have 25 mA totem-pole dividers and 1 k Ω terminators.

I/O Terminators — 220 Ω /330 Ω divider or 1 k Ω pullup.



Bus Drivers

Driver	Characteristic	Sink Current (mA)
Data	Tri-state	50
Address	Tri-state	50
Commands	Tri-state	32

Electrical Characteristics

Input Power

Frequency	Voltage
47-63 Hz	Standard — 115V AC $\pm$ 10%
	Option — 230V AC $\pm$ 10%

Output Power Available for Expansion Boards

Voltage	Supply Current	Without PROM ¹	With 4K PROM ²	With 8K PROM ³	Over Voltage Protection
+5	14A	10A	9.1A	8.8A	5.8 to 6.6V
+12	2A	1.91A	1.65A	1.91A	+14 to +16V
-5	0.9A	0.89A	0.72A	0.89A	-5.8 to -6.6V
-12	0.8A	0.78A	0.78A	0.78A	-14 to -16V

Notes

- Does not include power required for optional PROM, I/O drivers, and I/O terminators.
- With four 8708 EPROMs and 220 Ω /330 Ω input terminators installed for 32 I/O lines, all terminator inputs low.
- With four 8716 EPROMs and eight 220 Ω /330 Ω input terminators installed, all terminator inputs low.

Environmental Characteristics

Operating Temperature — 0°C to 55°C

Reference Manuals

9800484 — ISBC 80/20-4 Hardware Reference Manual
(SUPPLIED)

Reference manuals are shipped with each product only if designated SUPPLIED (see above). Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
Sys 80/20-4	System 80/20-4